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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,166	04/20/2001	Katsumi Ichinose	1095.1184	9022

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EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2127	3

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/838,166	ICHINOSE ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 6 are pending.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. **Claims 2, 5 and 6** are objected to because of the following informalities. Claims 2, 5 and 6 recite the limitations "said threads has been terminated" and "said threads has been processed", page 1, lines 5 – 6 and pages 3 – 4, lines 13 – 14, and lines 5 – 6, respectively. The Examiner believes these are grammatical errors.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1 – 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. **Claims 1, 3 and 4** recite the limitation "said thread" in page 1, line 16, page 2, line 17, and page 3, line 16, respectively. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1 – 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kametani (US 5,481,747).

9. Regarding **claim 1**, Kametani discloses an information processing method for causing a computing device having a plurality of processors to carry out predetermined information processing, the information processing method comprising:

a parallel processing block-forming step for diving a program to be executed into a plurality of parallel processing blocks (abstract, col. 12, lines 52 - 63);

a thread-forming step for dividing said parallel processing blocks formed by said parallel processing block-forming step, into threads which are basic units to be assigned respectively to said plurality of processors for being processed thereby (abstract, col. 12, lines 52 - 63); and

an instructing step for instructing a predetermined processor to execute a next parallel processing block when said predetermined processor has terminated execution of said thread assigned thereto (abstract, col. 2, lines 55 – 61, col. 4, line 66 – col. 5, line 19, col. 13, lines 22 – 26, col. 14, lines 36 - 49).

10. Regarding **claim 2**, Kametani discloses an information processing method according to claim 1, wherein when a predetermined instruction is given in said program to be executed, execution of a next parallel processing block is not instructed by said instructing step until processing of all of said threads have been terminated (abstract, col. 13, lines 27 – 31 and col. 14, lines 50 - 67).

11. **Claims 3 - 6** are rejected on the same ground as stated above.

12. Claims 1 – 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Applicants' admitted prior.

13. Regarding **claim 1**, Applicants' admitted prior art discloses an information processing method for causing a computing device having a plurality of processors to

carry out predetermined information processing, the information processing method comprising:

a parallel processing block-forming step for diving a program to be executed into a plurality of parallel processing blocks (specification page 1, lines 14 – 17, fig. 10);

a thread-forming step for dividing said parallel processing blocks formed by said parallel processing block-forming step, into threads which are basic units to be assigned respectively to said plurality of processors for being processed thereby (specification page 1, lines 14 – 20, fig. 10); and

an instructing step for instructing a predetermined processor to execute a next parallel processing block when said predetermined processor has terminated execution of said thread assigned thereto (specification page 2, lines 14 – 16, fig. 10).

14. Regarding **claim 2**, Applicants' admitted prior art discloses an information processing method according to claim 1, wherein when a predetermined instruction is given in said program to be executed, execution of a next parallel processing block is not instructed by said instructing step until processing of all of said threads have been terminated (specification page 2, lines 12 – 16, and page 6, line 1 – page 7, line 5).

15. **Claims 3 - 6** are rejected on the same ground as stated above.

16. Claims 1 – 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Muramatsu et al. (US 5,043,873, hereinafter Muramatsu).

17. Regarding **claim 1**, Muramatsu discloses an information processing method for causing a computing device having a plurality of processors to carry out predetermined information processing, the information processing method comprising:

a parallel processing block-forming step for diving a program to be executed into a plurality of parallel processing blocks (col. 1, lines 11 - 16);

a thread-forming step for dividing said parallel processing blocks formed by said parallel processing block-forming step, into threads which are basic units to be assigned respectively to said plurality of processors for being processed thereby (col. 1, lines 11 - 16); and

an instructing step for instructing a predetermined processor to execute a next parallel processing block when said predetermined processor has terminated execution of said thread assigned thereto (col. 3, lines 17 – 22, col. 14, line 55 – col. 15, line 3).

18. Regarding **claim 2**, Muramatsu discloses an information processing method according to claim 1, wherein when a predetermined instruction is given in said program to be executed, execution of a next parallel processing block is not instructed by said instructing step until processing of all of said threads have been terminated (col. 14, lines 22 - 54).

19. **Claims 3 - 6** are rejected on the same ground as stated above.

20. Claims 1 – 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Motomura (US 5,815,272).

21. Regarding **claim 1**, Motomura discloses an information processing method for causing a computing device having a plurality of processors to carry out predetermined information processing, the information processing method comprising:

a parallel processing block-forming step for diving a program to be executed into a plurality of parallel processing blocks (abstract, col. 1, lines 14 – 24, col. 2, lines 44 – 46, fig. 2);

a thread-forming step for dividing said parallel processing blocks formed by said parallel processing block-forming step, into threads which are basic units to be assigned respectively to said plurality of processors for being processed thereby (abstract, col. 1, lines 14 – 24, col. 2, lines 44 – 46, fig. 2); and

an instructing step for instructing a predetermined processor to execute a next parallel processing block when said predetermined processor has terminated execution of said thread assigned thereto (col. 26, lines 9 - 18).

22. Regarding **claim 2**, Muramatsu discloses an information processing method according to claim 1, wherein when a predetermined instruction is given in said program to be executed, execution of a next parallel processing block is not instructed by said instructing step until processing of all of said threads have been terminated (abstract, col. 2, lines 52 - 60).

23. **Claims 3 - 6** are rejected on the same ground as stated above.

24. Claims 1 and 3 – 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoki et al. (JP 2001167060, hereinafter Aoki).

25. Regarding **claim 1**, Aoki discloses an information processing method for causing a computing device having a plurality of processors to carry out predetermined information processing, the information processing method comprising:

a parallel processing block-forming step for diving a program to be executed into a plurality of parallel processing blocks (see translation in solution paragraph);

a thread-forming step for dividing said parallel processing blocks formed by said parallel processing block-forming step, into threads which are basic units to be assigned respectively to said plurality of processors for being processed thereby (see translation in solution paragraph); and

an instructing step for instructing a predetermined processor to execute a next parallel processing block when said predetermined processor has terminated execution of said thread assigned thereto (see translation in solution paragraph).

26. **Claims 3 - 5** are rejected on the same ground as stated above.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wakat et al. (US Pat. Application Publication 2002/0004966) disclosed the processor is executing the next ready task when it is done executing the current task.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 703-305-7864. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 703-305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2127

lv
April 14, 2004

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